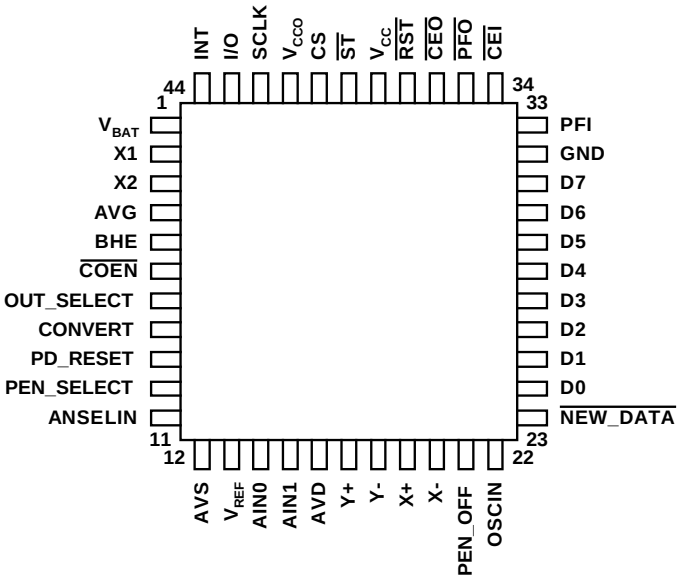
DS1680
Portable System Controller with Touch Screen Controller

FEATURES

- Provides Real Time Clock:
  - Counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100
  - Power control circuitry supports system power on from day/time alarm
- Microprocessor monitor:
  - Halts microprocessor during power–fail
  - Automatically restarts microprocessor after power failure
  - Monitors push–button for external override
  - Halts and resets an out of control microprocessor
- NV RAM control:
  - Automatic battery backup and write protection to external SRAM
- +5.0V operation
- 1.25V threshold detector for power–fail warning
- 10–bit analog–to–digital converter
  - Monotonic with no missing codes
- 4-wire analog resistive touch screen interface

PIN ASSIGNMENT



44-PIN QFP (10 mm x 10 mm)

ORDERING INFORMATION

DS1680FP-3	3.3V operation
DS1680FP-5	5.0V operation

DESCRIPTION

The DS1680 incorporates many of the functions necessary for low power portable products. The DS1680 provides a Real Time Clock, NV RAM controller, micro-processor monitor, power–fail warning, 10–bit analog–to–digital converter, and a touch screen controller.

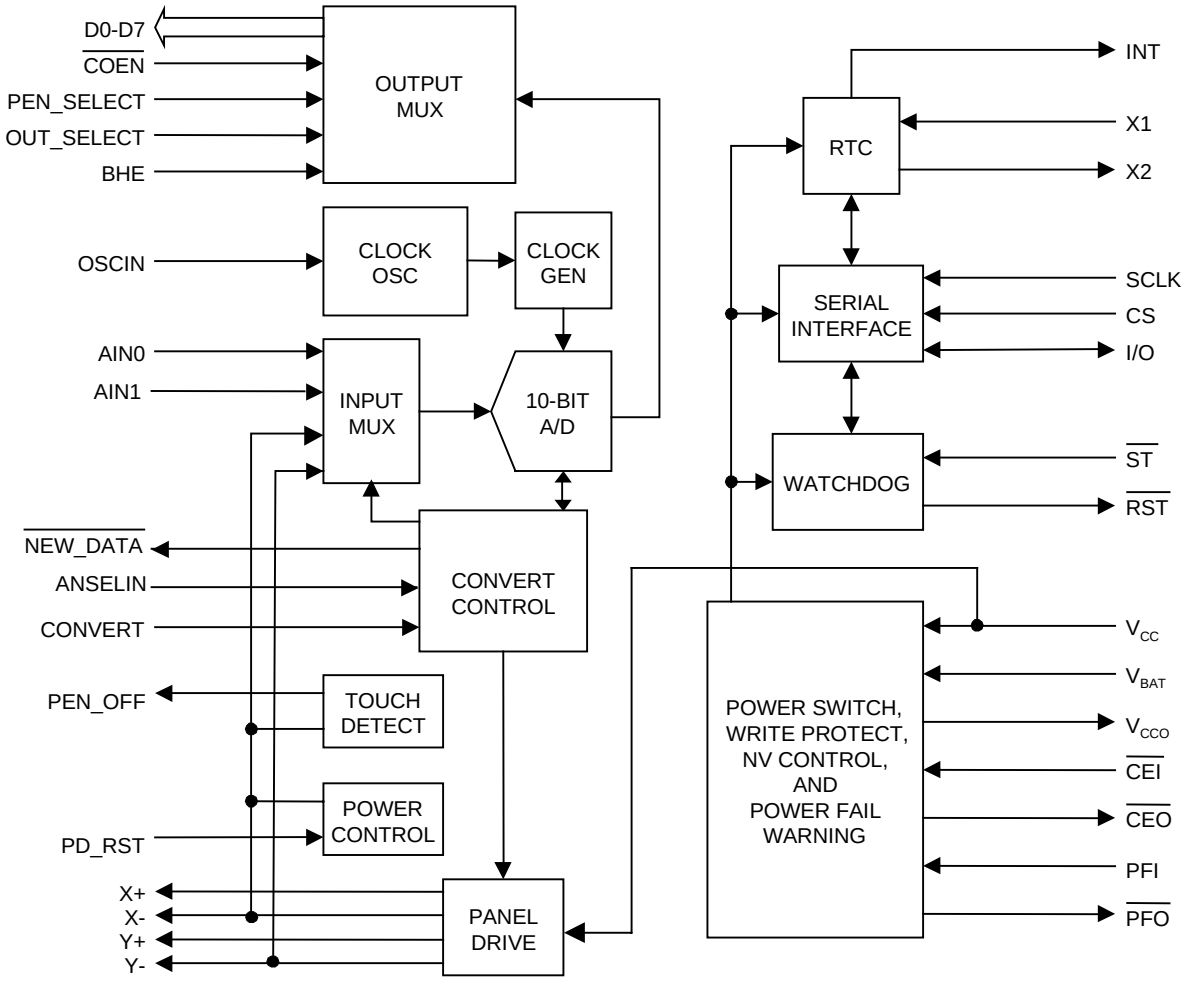
The Real Time Clock (RTC) provides seconds, minutes, hours, day, date, month, and year information with leap year compensation. The RTC also provides an alarm interrupt. This interrupt works when the DS1680 is powered by the system power supply or when in battery backup operation so the alarm can be used to wake up a system that is powered down.

Automatic backup and write protection of an external SRAM is provided through the V_{CCO} and $\overline{CEO}$ pins. The backup energy source used to power the RTC is also used to retain RAM data in the absence of V_{CC} through the V_{CCO} pin. The chip-enable output to SRAM, $\overline{CE0}$ **,** is controlled during power transients to prevent data corruption.

The microprocessor monitor circuitry of the DS1680 provides three basic functions. First, a precision temperature–compensated reference and comparator circuit monitors the status of V_{CC}. When an out–of–tolerance condition occurs, an internal power–fail signal is generated which forces $\overline{RST}$ to the active state. When V_{CC} returns to an in–tolerance condition, the $\overline{RST}$ signal is kept in the active state for t_{RPU} to allow the power supply and processor to stabilize. The DS1680 debounces a push–button input and guarantees an active $\overline{RST}$ pulse width of t_{RST}. The third function is a watchdog timer. The DS1680 has an internal timer that forces the $\overline{RST}$ signal to the active state if the strobe input is not driven low prior to watchdog time–out.

The DS1680 also provides a touch screen controller along with a 10–bit successive approximation analog–to–digital converter. The A/D converter is monotonic (no missing codes) and has an internal analog filter to reduce high frequency noise.

BLOCK DIAGRAM Figure 1



SIGNAL DESCRIPTIONS

V_{CC}, GND (Digital Supply and Digital Ground) – DC power to the RTC, watchdog, X, Y drivers, and power switching circuitry is provided to the device on these pins.

V_{BAT} (Backup Power Supply) – Battery input for standard 3-volt lithium cell or other energy source.

SCLK (Serial Clock Input) – SCLK is used to synchronize data movement on the serial interface.

I/O (Data Input/Output) – The I/O pin is the bi-directional data pin for the 3–wire interface.

CS (Chip Select) – The Chip Select signal must be asserted high during a read or a write for communication over the 3–wire serial interface.

V_{CCO} (External SRAM Power Supply Output) – This pin is internally connected to V_{CC} when V_{CC} is within nominal limits. However, during power–fail V_{CCO} is internally connected to the V_{BAT} pin. Switchover occurs when V_{CC} drops below V_{CCSW}.

INT (Interrupt Output) – The INT pin is an active high output of the DS1680 that can be used as an interrupt input to a microprocessor. The INT output remains high as long as the status bit causing the interrupt is present and the corresponding interrupt–enable bit is set. The INT pin operates when the DS1680 is powered by V_{CC} or V_{BAT}.

$\overline{\text{CEI}}$ (SRAM Chip Enable Input) – $\overline{\text{CEI}}$ must be driven low to enable the external SRAM.

$\overline{\text{CEO}}$ (SRAM Chip Enable Output) – Chip enable output for SRAM.

PFI (Power–Fail Input) – Power–Fail comparator input. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low; otherwise $\overline{\text{PFO}}$ remains high. Connect PFI to GND or V_{CC} when not used.

$\overline{\text{PFO}}$ (Power–Fail Output) – Power–Fail output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{\text{PFO}}$ remains high.

$\overline{\text{ST}}$ (Strobe Input) – The Strobe input pin is used in conjunction with the watchdog timer. If the $\overline{\text{ST}}$ pin is not driven low within the watchdog time period, the $\overline{\text{RST}}$ pin is driven low.

$\overline{\text{RST}}$ (Reset) – The $\overline{\text{RST}}$ pin functions as a microprocessor reset signal. This pin has an internal 47 kΩ pull up resistor.

X1, X2 – Connections for a standard 32.768 kHz quartz crystal. For greatest accuracy, the DS1680 must be used with a crystal that has a specified load capacitance of 6 pF. There is no need for external capacitors or resistors. Note: X1 and X2 are very high impedance nodes. It is recommended that they and the crystal be guard–ringed with ground and that high frequency signals be kept away from the crystal area. For more information on crystal selection and crystal layout considerations, please consult Application Note 58, “Crystal Considerations with Dallas Real Time Clocks”. The DS1680 will not function without a crystal.

AVD, AVS (A/D Supply and Ground) – Power supply and ground for the A/D.

AIN0, AIN1, (Analog Inputs) – These pins are the analog inputs for the A/D converter.

V_{REF} (Voltage Reference) – Reference voltage for the A/D.

X+, X- (Resistive Tablet X Plane Driver) – Connect to X-terminal of resistive tablet.

Y+, Y- (Resistive Tablet Y Plane Driver) – Connect to Y-terminal of resistive tablet.

CONVERT - Assert to logic 1 to request sample from AIN0 or AIN1. Use with ANSELIN input.

ANSELIN (Analog Select Input) - Assert to logic 0 to select AIN0. Assert to logic 1 to select AIN1. Use with CONVERT input.

BHE (Bus High Enable Input) - Drive to logic 1 to select high byte (data bits 2-9). Drive to logic 0 to select low byte (data bits 0-1). The lower 6 bits will all be zeros when asserted low.

PEN_SELECT (Pen Select Input) - Assert to logic 1 to select X- or Y- data output. Assert to logic 0 to select AIN0 or AIN1 data output. Use with OUT_SELECT input.

OUT_SELECT (Output Select Input) - Assert to logic 0 to select AIN0 or X- data. Assert to logic 1 to select AIN1 or Y- data. Use with PEN_SELECT input.

$\overline{\text{COEN}}$ (Chip Output Enable) - The $\overline{\text{COEN}}$ pin must be asserted low to enable the A/D data to be read on D0-D7.

D0-D7 (Data Bus) – Data output from A/D.

AVG (Data Average Select Pin) – Logic 1 selects data average mode. Logic 0 selects raw data mode.

$\overline{\text{NEW\_DATA}}$ (New Data Indicator) – A logic 0 pulse indicates that new data packet is available on D0-D7.

OSCIN (Oscillator Input) – Input for the A/D clock.

PEN_OFF (Pen Detection Output) – Indicates pen not detected. Logic 1 if pen is not detected.

PD_RESET (Power Down/Reset Input) – Assert Logic 1 for ≥ 10 ns to reset. Hold at Logic 1 for power-down mode of the analog circuitry.

3–WIRE SERIAL INTERFACE

Communication with the RTC and watchdog is accomplished through a simple 3–wire interface consisting of the Chip Select (CS), Serial Clock (SCLK) and Input/Output (I/O) pins.

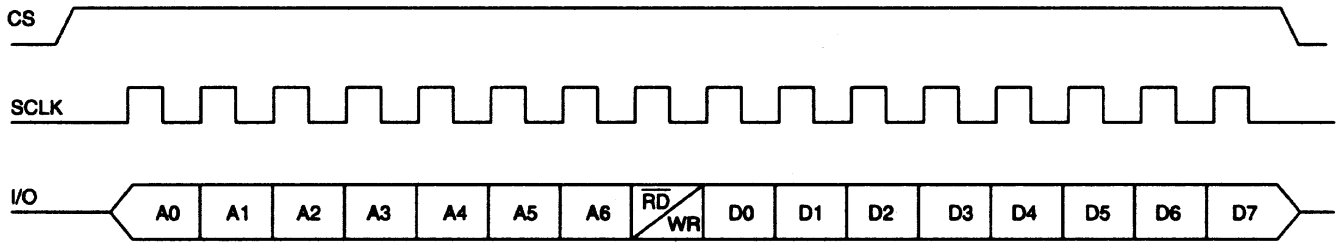
All data transfers are initiated by driving the CS input high. The CS input serves two functions. First, CS turns on the control logic, which allows access to the shift register for the address/command sequence. Second, the CS signal provides a method of terminating either single byte or multiple byte (burst) data transfer. A clock cycle is a sequence of a rising edge followed by a falling edge. For data input, data must be valid during the rising edge of the clock and data bits are output on the falling edge of the clock. If the CS input goes low, all data transfer terminates and the I/O pin goes to a high impedance state.

Address and data bytes are always shifted LSB first into the I/O pin. Any transaction requires the address/command byte to specify a read or write to a specific register followed by one or more bytes of data. The address byte is always the first byte entered after CS is driven high. The most significant bit ($\overline{RD}$/WR) of this byte determines if a read or write will take place. If this bit is 0, one or more read cycles will occur. If this bit is 1, one or more write cycles will occur.

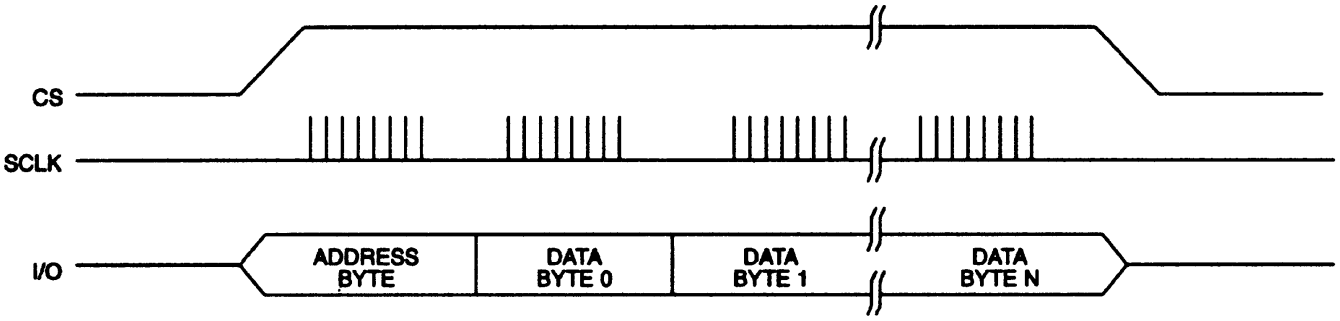
Data transfers can occur one byte at a time or in multiple byte burst mode. After CS is driven high an address is written to the DS1680. After the address, one or more data bytes can be read or written. For a single byte transfer one byte is read or written and then CS is driven low. For a multiple byte transfer, multiple bytes can be read or written to the DS1680 after the address has been written. Each read or write cycle causes the register address to automatically increment. Incrementing continues until the device is disabled. After accessing register 0 Dh, the address wraps to 00h.

Data transfer for single byte transfer and multiple byte burst transfer is illustrated in Figures 2 and 3.

SINGLE BYTE DATA TRANSFER Figure 2



MULTIPLE BYTE BURST TRANSFER Figure 3



ADDRESS/COMMAND BYTE

The command byte for the DS1680 is shown in Figure 4. Each data transfer is initiated by a command byte. Bits zero through six specify the address of the registers to be accessed. The MSB (bit 7) is the Read/Write bit. This bit specifies whether the accessed byte will be read or written. A read operation is selected if bit 7 is a zero and a write operation is selected if bit 7 is a one. The address map for the DS1680 is shown in Figure 5.

ADDRESS/COMMAND BYTE Figure 4

7	6	5	4	3	2	1	0
$\overline{RD}$ / WR	A6	A5	A4	A3	A2	A1	A0

RTC/WATCHDOG ADDRESS MAP Figure 5

	BIT7							BIT0
00	0	10 SECONDS			SECONDS			
01	0	10 MINUTES			MINUTES			
02	0	12/24	10 HR A/P	10 HR	HOURS			
03	0	0	0	0	0	DAY		
04	0	0	10 DATE		DATE			
05	0	0	0	10 MO.	MONTH			
06	10 YEAR				YEAR			
07	M	10 SEC ALARM			SECONDS ALARM			
08	M	10 MIN ALARM			MINUTES ALARM			
09	M	12/24	10 HR A/P	10 HR	HOUR ALARM			
0A	M	0	0	0	0	DAY ALARM		
0B	CONTROL REGISTER							
0C	STATUS REGISTER							
0D	WATCHDOG REGISTER							
0E	RESERVED							
7F								

CLOCK, CALENDAR AND ALARM

The time and calendar information is accessed by reading/writing the appropriate register bytes. Note that some bits are set to zero. These bits will always read zero regardless of how they are written. Also note that registers 0 Eh to 7 Fh are reserved. These registers will always read zero regardless of how they are written. The contents of the time, calendar, and alarm registers are in the Binary–Coded Decimal (BCD) format.

The DS1680 can run in either 12–hour or 24–hour mode. Bit 6 of the hours register is defined as the 12– or 24–hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic one being PM. In the 24–hour mode, bit 5 is the second 10–hour bit (20–23 hours).

The DS1680 also contains a time of day alarm. The alarm registers are located in registers 07h to 0 Ah. Bit 7 of each of the alarm registers are mask bits (see Table 1). When all of the mask bits are logic 0, an alarm will occur once per week when the values stored in time-keeping registers 00h to 03h match the values stored in the time of day alarm registers. An alarm will be generated every day when mask bit of the day alarm register is set to one. An alarm will be generated every hour when the day and hour alarm mask bits are set to one. Similarly, an alarm will be generated every minute when the day, hour, and minute alarm mask bits are set to one. When day, hour, minute and seconds alarm mask bits are set to one, an alarm will occur every second.

TIME OF DAY ALARM BITS Table 1

ALARM REGISTER MASK BITS (BIT 7)				
SECONDS	MINUTES	HOURS	DAY	
1	1	1	1	Alarm once per second.
0	1	1	1	Alarm when seconds match.
0	0	1	1	Alarm when minutes and seconds match.
0	0	0	1	Alarm when hours, minutes and seconds match.
0	0	0	0	Alarm when day, hours, minutes and seconds match.

SPECIAL PURPOSE REGISTERS

The DS1680 has two additional registers (control register and status register) that control the Real Time Clock and interrupts.

CONTROL REGISTER – 0Bh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{\text{EOSC}}$	WP	SP1	SP0	0	0	0	AIE

$\overline{\text{EOSC}}$ (Enable oscillator) – This bit, when set to logic 0 will start the oscillator. When this bit is set to a logic 1, the oscillator is stopped and the DS1680 is placed into a low–power standby mode (I_{BAT}) when in battery back–up mode. When the DS1680 is powered by V_{CC}, the oscillator is always on regardless of the status of the $\overline{\text{EOSC}}$ bit; however, the real time clock is incremented only when $\overline{\text{EOSC}}$ is a logic 0.

SP0 and SP1 (Speed select) – These bits select the on time of the "X" and "Y" measurement duty cycle. The Programmable Duty Cycle section has more detail.

WP (Write Protect) – Before any write operation to the real time clock or any other registers, this bit must be logic 0. When high, the write protect bit prevents a write operation to any register.

AIE (Alarm Interrupt Enable) – When set to a logic 1, this bit permits the Interrupt Request Flag (IRQF) bit in the status register to assert INT. When the AIE bit is set to logic 0, the IRQF bit does not initiate the INT signal.

STATUS REGISTER – 0Ch

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	LOBAT	0	0	0	0	0	IRQF

LOBAT (Low Battery Flag) – This bit reflects the status of the backup power source connected to the V_{BAT} pin. When V_{BAT} is greater than 2.5 volts, LOBAT is set to a logic 0. When V_{BAT} is less than 2.3 volts, LOBAT is set to a logic 1.

IRQF (Interrupt Request Flag) – A logic 1 in the Interrupt Request Flag bit indicates that the current time has matched the time of day Alarm registers. If the AIE bit is also a logic 1, the INT pin will go high. IRQF is cleared by reading or writing to any of the alarm registers.

POWER–UP/POWER–DOWN CONSIDERATIONS

When V_{CC} is applied to the DS1680 and reaches a level greater than V_{CCTP} (trip point), the device becomes fully accessible after t_{RPU} (250 ms typical). Before t_{RPU} elapses, some inputs are disabled. When V_{CC} drops below V_{CCSW}, the device is switched over to the V_{BAT} supply.

During power–up, when V_{CC} returns to an in–tolerance condition, the $\overline{RST}$ pin is kept in the active state for 250 ms (typical) to allow the power supply and microprocessor to stabilize.

NONVOLATILE SRAM CONTROLLER

The DS1680 provides automatic backup and write protection for an external SRAM. This function is provided by gating the chip enable signal and by providing a constant power supply through the V_{CCO} pin.

The DS1680 nonvolatizes the external SRAM by write protecting the SRAM and by providing a back–up power supply in the absence of V_{CC}. When V_{CC} falls below V_{CCTP}, access to the external SRAM is prohibited by forcing $\overline{CE0}$ high regardless of the level of $\overline{CEI}$. Upon power–up, access is prohibited until the end of t_{RPU}.

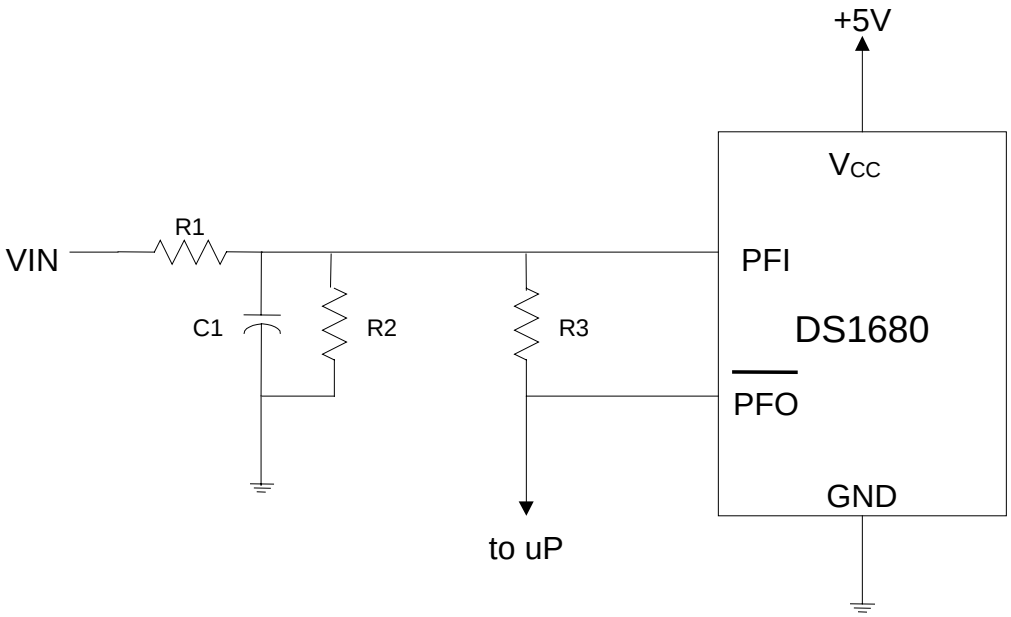
POWER–FAIL COMPARATOR

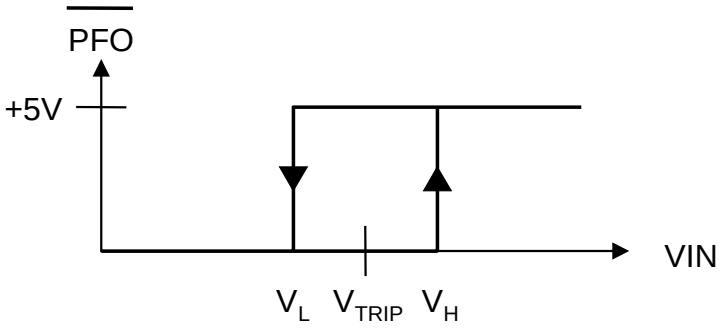
The PFI input is connected to an internal reference. If PFI is less than 1.25V, $\overline{PFO}$ goes low. The power–fail comparator can be used as an undervoltage detector to signal an impending power supply failure. $\overline{PFO}$ can be used as a μP interrupt input to prepare for power–down. For battery conservation, the comparator is turned off and $\overline{PFO}$ is held low when in battery–backed mode

ADDING HYSTERESIS TO THE POWER–FAIL COMPARATOR

Hysteresis adds a noise margin to the power–fail comparator and prevents $\overline{PFO}$ from oscillating when VIN is near the power–fail comparator trip point. Figure 6 shows how to add hysteresis to the power–fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistors R2 and R3 adds hysteresis. R3 will typically be an order of magnitude greater than R1 or R2. R3 should be chosen in manner to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds noise filtering and has a value of typically 1.0 uF. See Figure 6 for a schematic diagram and equations.

POWER–FAIL COMPARATOR Figure 6





$$V_{TRIP} = 1.25 \left(\frac{R1 + R2}{R2} \right) \qquad V_H = 1.25 / \left(\frac{R2||R3}{R1 + R2||R3} \right)$$

$$\frac{V_L - 1.25}{R1} + \frac{5 - 1.25}{R3} = \frac{1.25}{R2}$$

MICROPROCESSOR MONITOR

The DS1680 monitors three vital conditions for a micro-processor: power supply, software execution, and external override.

First, a precision temperature–compensated reference and comparator circuit monitors the status of V_{CC}. When an out–of–tolerance condition occurs, an internal power–fail signal is generated which forces the $\overline{RST}$ pin to the active state thus warning a processor–based system of impending power failure. When V_{CC} returns to an in–tolerance condition upon power–up, the reset signal is kept in the active state for t_{RST} to allow the power supply and microprocessor to stabilize. Note however that if the $\overline{EOSC}$ bit is set to a logic 1 (to disable the oscillator during battery back–up mode), the $\overline{RST}$ signal will be kept in an active state for t_{RST} plus the start–up time of the oscillator.

The second monitoring function is push-button reset control. The DS1680 provides for a push–button switch to be connected to the $\overline{RST}$ output pin. When the DS1680 is not in a reset cycle, it continuously monitors the $\overline{RST}$ signal for a low going edge. If an edge is detected, the DS1680 will debounce the switch by pulling the $\overline{RST}$ line low. After the internal timer has expired, the DS1680 will continue to monitor the $\overline{RST}$ line. If the line is still low, the DS1680 will continue to monitor the line looking for a rising edge. Upon detecting release, the DS1680 will force the $\overline{RST}$ line low and hold it low for t_{RST}.

The third microprocessor monitoring function provided by the DS1680 is a watchdog timer. The watchdog timer function forces $\overline{RST}$ to the active state when the $\overline{ST}$ input is not stimulated within the predetermined time period. The time period is set by the Time Delay (TD) bits in the Watchdog Register. The time delay can be set to 250 ms, 500 ms, or 1000 ms. If TD0 and TD1 are both set to zero, the watchdog timer is disabled. When enabled, the watchdog timer starts timing out from the set time period as soon as $\overline{RST}$ is inactive. The default setting is for the watchdog timer to be enabled with 1000 ms time delay. If a high–to–low transition occurs on the $\overline{ST}$ input pin prior to time–out, the watchdog timer is reset and begins to time–out again. If the watchdog timer is allowed to time–out, then the $\overline{RST}$ signal is driven to the active state for t_{RST}. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. To guarantee that the watchdog timer does not time–out, a high–to–low transition must occur at or less than the minimum period.

WATCHDOG REGISTER – 0Dh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	TD1	TD0

WATCHDOG TIME-OUT BITS Table 2

TD1	TD0	WATCHDOG TIME-OUT
0	0	WATCHDOG DISABLED
0	1	250 ms
1	0	500 ms
1	1	1000 ms

RESISTIVE TOUCH SCREEN (4-WIRE)

Resistive touch screens consist of 2 resistive plates that are separated by a small gap. Each plate has an electrode at each end and when the screen is touched, the pressure forces the two plates to come in contact at the exact position of the touch. To get the x-coordinate position, the DS1680 will drive the X-plane resistive film (via X+ and X-) and sense the voltage picked up by the Y-plane resistive film (via Y+ and Y-). Next, to get the y-coordinate position, the DS1680 will drive the Y- plane resistive film and sense the voltage picked up by the X-plane resistive film.

ANALOG–TO–DIGITAL CONVERTER

The DS1680 provides a 10–bit analog–to–digital converter. Two multiplexed analog inputs are provided through the AIN0 and AIN1 pins along with two other inputs on the X- and Y- pins. The A/D converter is monotonic (no missing codes) and uses a successive approximation technique to convert the analog signal into a digital code.

An A/D conversion is the process of assigning a digital code to an analog input voltage. This code represents the input value as a fraction of the full-scale voltage (FSV) range. Thus the FSV range is then divided by the A/D converter into 1024 codes (10 bits). The FSV range is bounded by an upper limit equal to the reference voltage and the lower limit, which is ground.

On chip circuitry detects if the pen is in contact with the digitizer tablet. The pen-detection status is indicated on pin (PEN_OFF) and may be used by the system for signaling end-of-stroke for handwriting recognition software purposes. If no pen is detected, PEN_OFF will be pulled to logic 1 and no coordinate data will be made available. PEN_OFF at logic 0 indicates that a pen is detected on the digitizer tablet and its coordinate position will be made available on D0-D7. The NEW_DATA pin pulses low to indicate when a new coordinate data pair is available.

When the AVG pin is set to logic 0, the data at pins D0-D7 will indicate the most recent sample by the A/D. When the AVG pin is set to logic 1, the data averaging mode is invoked. In this mode, the data output on D0-D7 will indicate the rolling average of the four most recent samples of the A/D.

The CONVERT signal can also be used to request a sample from the AIN0 or AIN1 inputs. Whenever a logic 1 is asserted on CONVERT, a reading will be taken on either the AIN0 or AIN1 input along with a reading of the X, Y coordinates. The logic level of the ANSELIN input will determine whether a sample is taken from the AIN0 or AIN1 input. Table 3 lists the specific analog input that is selected by these two signals. The CONVERT signal can be used regardless of the status of the PEN_OFF signal. Depending on when in the conversion cycle the CONVERT request is initiated, the output may not be available until the next cycle. Thus it is suggested that you read the output twice whenever using the CONVERT signal.

ANALOG INPUT SELECTION Table 3

CONVERT	ANSELIN	ANALOG INPUT(S)
0	0	X-, Y-
0	1	X-, Y-
1	0	X-, Y-, AIN0
1	1	X-, Y-, AIN1

PROGRAMMABLE DUTY CYCLE

The current required to take an 'X' or 'Y' measurement is V_{AVD}/R_D. In the case of R_D = 250 ohms and V_{AVD}=5V the current required is 20 mA. The average current is the current during the measurement, multiplied by the ratio of the time the drivers are on, to the total sample time. In order to minimize the average current, the on time should be limited to the minimum time required for the tablet RC delay.

Experimental data suggests that a typical RC time constant is between 4 and 5 µs for a resistive touch screen. In order to achieve 10 bit resolution, the settling time must be 8 time constants. This creates a requirement of a minimum of 80 µs on-time total, 40 µs for each 'X' and 'Y' measurement.

In order to provide both low power and high sample rate, the on time for the 'X' and 'Y' measurement duty cycle is programmable. Bits 4 and 5 (SP0 and SP1) of the control register (0Bh) select the on time of 4 different frequency ranges. The frequencies given are the maximum frequency, for that timing range, which will not violate the 40 µs per measurement requirement.

SP1	SP0	Frequency Range	Average Current	Samples/Sec	# of Cycles
0*	0*	2.0 MHz	870 uA	543	5
0	1	2.8 MHz	1.217 mA	760	7
1	0	4.0 MHz	1.739 mA	1086	10
1	1	5.0 MHz	2.261 mA	1359	13

*This is the default setting

Average current is the current required for the measurement, averaged out over the entire sample. This average current is only related to the measurement phase when the drivers are on. The average current will be drawn from the V_{CC} supply. There is also current associated with the pen detection phase, the ADC, and the control logic.

The # of cycles indicated is the number of on-time state cycles. 1 state cycle is 16 main clock cycles. If the frequency range is 2.0 MHz, the state frequency is 2 MHz/16 = 125 kHz. There are 230 state cycles in one complete sample. The number of cycles can be used to calculate the settling time and the sample rate.

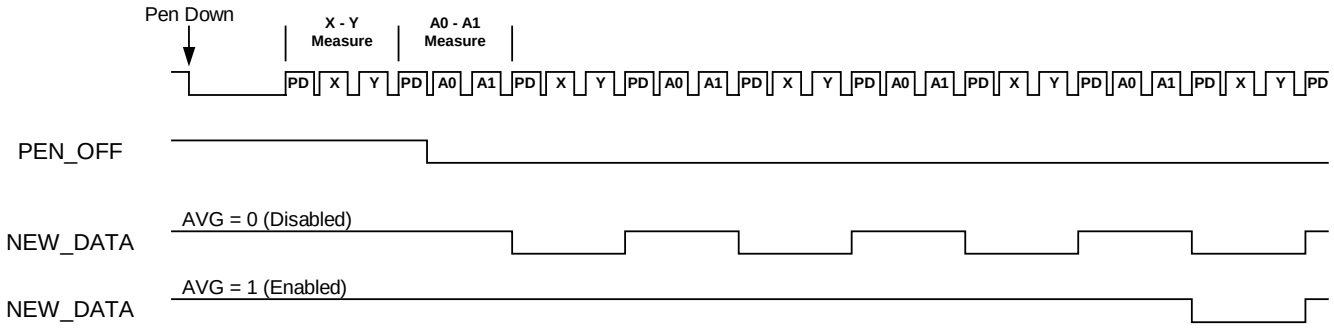
Example 1:

Frequency Range : 2.0 MHz
Clock Frequency : 1.8432 MHz
tsettle = (1/1.8432e6)*16*5 = 43.4 µs
Iavg = (10/230)*20 mA = 870 µA
Sample Rate = 1.8432e6/(16*230) = 501 samples/sec

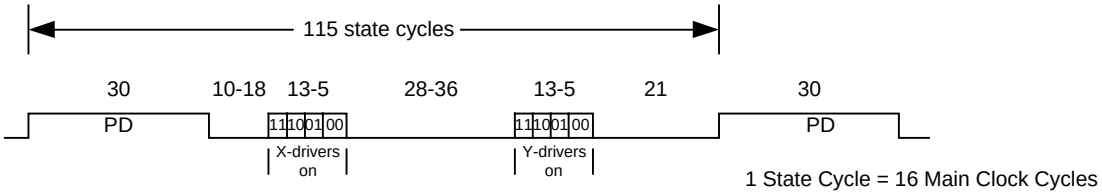
Example 2:

Frequency Range : 2.8 MHz
Clock Frequency : 1.8432 MHz
tsettle = (1/1.8432e6)*16*7 = 60.8 µs
Iavg = (14/230)/*20 mA = 1.217 mA
Sample Rate = 1.8432e6/(16*230) = 501 samples/sec

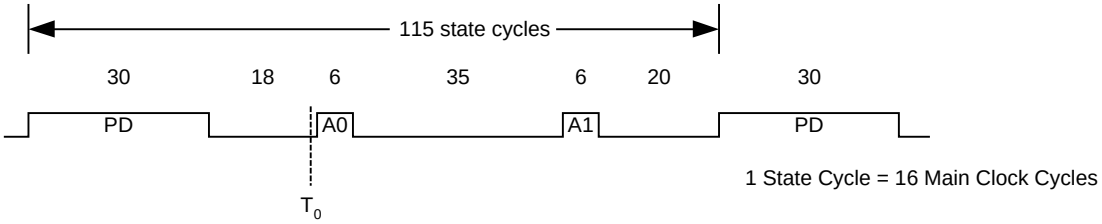
CONVERSION TIMING Figure 7a



X - Y Meas Figure 7b



AIN0 - AIN1 Meas Figure 7c



NOTE:

If the CONVERT signal is asserted before T_0, AIN0 and/or AIN1 will be sampled and converted in the present conversion cycle; otherwise the AIN0 and/or AIN1 signals will be sampled and converted in the next conversion cycle.

PARRALLEL INTERFACE

The A/D output is available on the data bus at pins D0-D7. A logic 0 on $\overline{\text{COEN}}$ will enable data onto the data bus so that the DS1680 may be used in parallel with other devices. PEN_SELECT and OUT_SELECT are used to decode which analog output (X-, Y-, AIN0, or AIN1) is output on the data bus when $\overline{\text{COEN}}$ is asserted low. Since the device offers 10-bit resolution, the BHE pin is used to decode the 10 bits of data on the data bus. A logic 1 on BHE will enable data bits B2-B9. A logic 0 will enable data bits B0-B1 along with the six LSBs=0. The status pin ($\overline{\text{NEW\_DATA}}$) pulses low to indicate that new coordinate or conversion is available. The output can be read while $\overline{\text{NEW\_DATA}}$ is low or after it has gone high**.** Output selection and parallel data format is shown below.

OUTPUT SELECTION Table 4

PEN_SELECT	OUT_SELECT	ANALOG OUTPUT
0	0	AIN0
0	1	AIN1
1	0	X-
1	1	Y-

PARALLEL DATA FORMAT

		MSB							LSB
High Byte	BHE=1	B9	B8	B7	B6	B5	B4	B3	B2
Low Byte	BHE=0	B1	B0	0	0	0	0	0	0

POWER MANAGEMENT (A/D AND PEN-INPUT PROCESSOR)

The DS1680 analog circuitry can be placed into a low power mode by asserting and holding the PD_RESET pin at logic 1. Normal operation will resume when PD_RESET is returned to logic 0.

To further conserve power, the pen-detection circuitry will automatically switch the analog circuitry to power down mode whenever there is no pen input detected for more than three seconds. Normal operation will automatically resume when any one of the following three events occur: pen down is detected; the CONVERT signal is activated; or chip is reset (PD_RESET pulled to logic 1 and then returned to logic 0.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–55°C to +125°C
Soldering Temperature	See J-STD-020A specification

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Digital Power Supply Voltage 3.3V Operation	V_{CC}, V_{AVD}, V_{REF}	3.0	3.3	3.6	V	1
Digital Power Supply Voltage 5V Operation	V_{CC}, V_{AVD}, V_{REF}	4.5	5.0	5.5	V	1
Input Logic 1	V_{IH}	2.0		V_{CC}+0.3	V	1
Input Logic 0	V_{IL}	-0.3		+0.8	V	1
Battery Voltage	V_{BAT}	2.5		3.7	V	1

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
CS Leakage	I_{LO}			150	µA	8
Logic 1 Output	V_{OH}	2.4			V	2
Logic 0 Output	V_{OL}			0.4	V	3
Active Supply Current (No Pen Detect)	I_{CCA}		1.5	2.0	mA	4
Active Supply Current (Pen Detected)	I_{CCPD}			5	mA	20
Standby Current	I_{CCS}			300	µA	5
Oscillator Current	I_{OSC}		300	500	nA	18
Battery Current (Oscillator Off)	I_{BAT}			200	nA	19
Internal RST Pull-Up Resistor	R_P	35	47	60	kΩ	
V_{CC} Trip Point	V_{CCTP}	4.25	4.35	4.50	V	
V_{CC} Switchover	V_{CCSW}	2.60	2.70	2.80	V	13
Pushbutton Detect	PB_{DV}	0.8		2.0	V	
Pushbutton Release	PB_{RD}		0.3	0.8	V	
Output Voltage	V_{CCO}	V_{CC}-0.3			V	12
V_{CCO} Output Current (Source=V_{CC})	I_{CCO1}			150	mA	14
V_{CCO} Output Current (Source=V_{BAT})	I_{CCO2}			150	µA	15
PFI Input Threshold	V_{PFI}	1.20	1.25	1.30	V	
PFI Input Current	I_{PFI}	0.25		25	nA	
$\overline{PFO}$ Output Voltage, I_{OH} = -1 µA	V_{OH}	V_{CC}-1.5			V	
$\overline{PFO}$ Output Voltage, I_{OL} = 3.2 µA	V_{OL}			0.4	V	

DC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=3.3V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage	I_{LI}	-1		+1	µA	
CS Leakage	I_{LO}			150	µA	8
Logic 1 Output	V_{OH}	2.4			V	2
Logic 0 Output	V_{OL}			0.4	V	3
Active Supply Current (No Pen Detect)	I_{CCA}		0.75	1.0	mA	4
Active Supply Current (Pen Detected)	I_{CCPD}			3	mA	20
Standby Current	I_{CCS}			100	µA	5
Oscillator Current	I_{OSC}		300	500	nA	18
Battery Current (Oscillator Off)	I_{BAT}			200	nA	19
Internal RST Pull-Up Resistor	R_P	35	47	60	kΩ	
V_{CC} Trip Point	V_{CCTP}	2.80	2.88	2.97	V	
V_{CC} Switchover	V_{CCSW}	2.62	2.70	2.78	V	13
Pushbutton Detect	PB_{DV}	0.8		2.0	V	
Pushbutton Release	PB_{RD}		0.3	0.8	V	
Output Voltage	V_{CCO}	V_{CC}-0.3			V	12
V_{CCO} Output Current (Source=V_{CC})	I_{CCO1}			80	mA	14
V_{CCO} Output Current (Source=V_{BAT})	I_{CCO2}			100	µA	15
PFI Input Threshold	V_{PFI}	1.20	1.25	1.30	V	
PFI Input Current	I_{PFI}	0.25		25	nA	
$\overline{PFO}$ Output Voltage, I_{OH} = -1 µA	V_{OH}	V_{CC}-1.5			V	
$\overline{PFO}$ Output Voltage, I_{OL} = 3.2 µA	V_{OL}			0.4	V	

CAPACITANCE (t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_I		10		pF	
I/O Capacitance	$C_{I/O}$		15		pF	
Crystal Capacitance	C_X		6		pF	

3-WIRE INTERFACE

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to Clock Setup	t_{DC}	50			ns	9
CLK to Data Hold	t_{CDH}	70			ns	9
CLK to Data Delay	t_{CDD}			200	ns	9, 10, 11
CLK to Low Time	t_{CL}	250			ns	9
CLK to High Time	t_{CH}	250			ns	9
CLK Frequency	t_{CLK}			2.0	MHz	9
CLK Rise and Fall	t_R, t_F			500	ns	
CS to CLK Setup	t_{CC}	1			µs	9
CLK to CS Hold	t_{CCH}	60			ns	9
CS Inactive Time	t_{CWH}	1			µs	9
CS to I/O High-Z	t_{CDZ}			70	ns	9
V_{CC} Slew Rate (4.5V to 2.3V)	t_F	1			ms	
V_{CC} Slew Rate (2.3V to 4.5V)	t_R	0			ns	

3-WIRE INTERFACE

AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=3.3V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data to Clock Setup	t_{DC}	150			ns	9
CLK to Data Hold	t_{CDH}	210			ns	9
CLK to Data Delay	t_{CDD}			600	ns	9, 10, 11
CLK to Low Time	t_{CL}	750			ns	9
CLK to High Time	t_{CH}	750			ns	9
CLK Frequency	t_{CLK}			0.667	MHz	9
CLK Rise and Fall	t_R, t_F			1500	ns	
CS to CLK Setup	t_{CC}	3			µs	9
CLK to CS Hold	t_{CCH}	180			ns	9
CS Inactive Time	t_{CWH}	3			µs	9
CS to I/O High-Z	t_{CDZ}			210	ns	9
V_{CC} Slew Rate (4.5V to 2.3V)	t_F	300			ms	
V_{CC} Slew Rate (2.3V to 4.5V)	t_R	0			ns	

A/D CHARACTERISTICS (0°C to 70°C; V_{CC}, V_{AVD}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Resistance of Digitizer Film	R_D	250	600	1000	Ω	
Resistance of on chip Driver	R_{DRIVER}		12	25	Ω	
Parasitic Capacitance between X and Y-plates of Digitizer	C_{XY}		5	10	nF	
Ladder Resistance	R_{REF}	11	19	27	kΩ	
A/D Active Current	I_{AVDA}			TBD	µA	6
A/D Standby Current	I_{AVDS}			TBD	µA	7
Reference Current	I_{REF}			300	µA	
Input Leakage (AIN0, AIN1)	I_{LI}		10		nA	
Analog Input Capacitance	C_{IN}		10	15	pF	
Resolution			10		Bits	
Differential non-linearity	E_{DL}		± 0.5	± 1.0	LSB	
Integral non-linearity	E_{IL}		± 0.5	± 1.0	LSB	
Offset Error	E_{OS}		± 1.0	± 1.5	LSB	
Gain Error	E_G		± 0.25	± 1.0	%	
A/D Clock Frequency	F_{OSCIN}		1.8432	5.0	MHz	
Multiplexer selector path propagation delay	t_{MUX}			60	ns	
$\overline{COEN}$ falling edge to data bus driven	t_{OEA}			40	ns	
$\overline{COEN}$ rising edge to data bus Hi-Z	t_{OEZ}			40	ns	

A/D CHARACTERISTICS

(0°C to 70°C; V_{CC}, V_{AVD}=3.3V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Resistance of Digitizer Film	R_D	250	600	1000	Ω	
Resistance of on chip Driver	R_{DRIVER}		15	30	Ω	
Parasitic Capacitance between X and Y-plates of Digitizer	C_{XY}		5	10	nF	
Ladder Resistance	R_{REF}	11	19	27	kΩ	
A/D Active Current	I_{AVDA}			TBD	µA	6
A/D Standby Current	I_{AVDS}			TBD	µA	7
Reference Current	I_{REF}			200	µA	
Input Leakage (AIN0, AIN1)	I_{LI}		10		nA	
Analog Input Capacitance	C_{IN}		10	15	pF	
Resolution			10		Bits	
Differential non-linearity	E_{DL}		± 0.5	± 1.0	LSB	
Integral non-linearity	E_{IL}		± 0.5	± 1.0	LSB	
Offset Error	E_{OS}		± 1.0	± 1.5	LSB	
Gain Error	E_G		± 0.25	± 1.0	%	
A/D Clock Frequency	F_{OSCIN}			2.5	MHz	
Multiplexer selector path propagation delay	t_{MUX}			120	ns	
$\overline{COEN}$ falling edge to data bus driven	t_{OEA}			80	ns	
$\overline{COEN}$ rising edge to data bus Hi-Z	t_{OEZ}			80	ns	

POWER-FAIL AND RESET AC ELECTRICAL CHARACTERISTICS

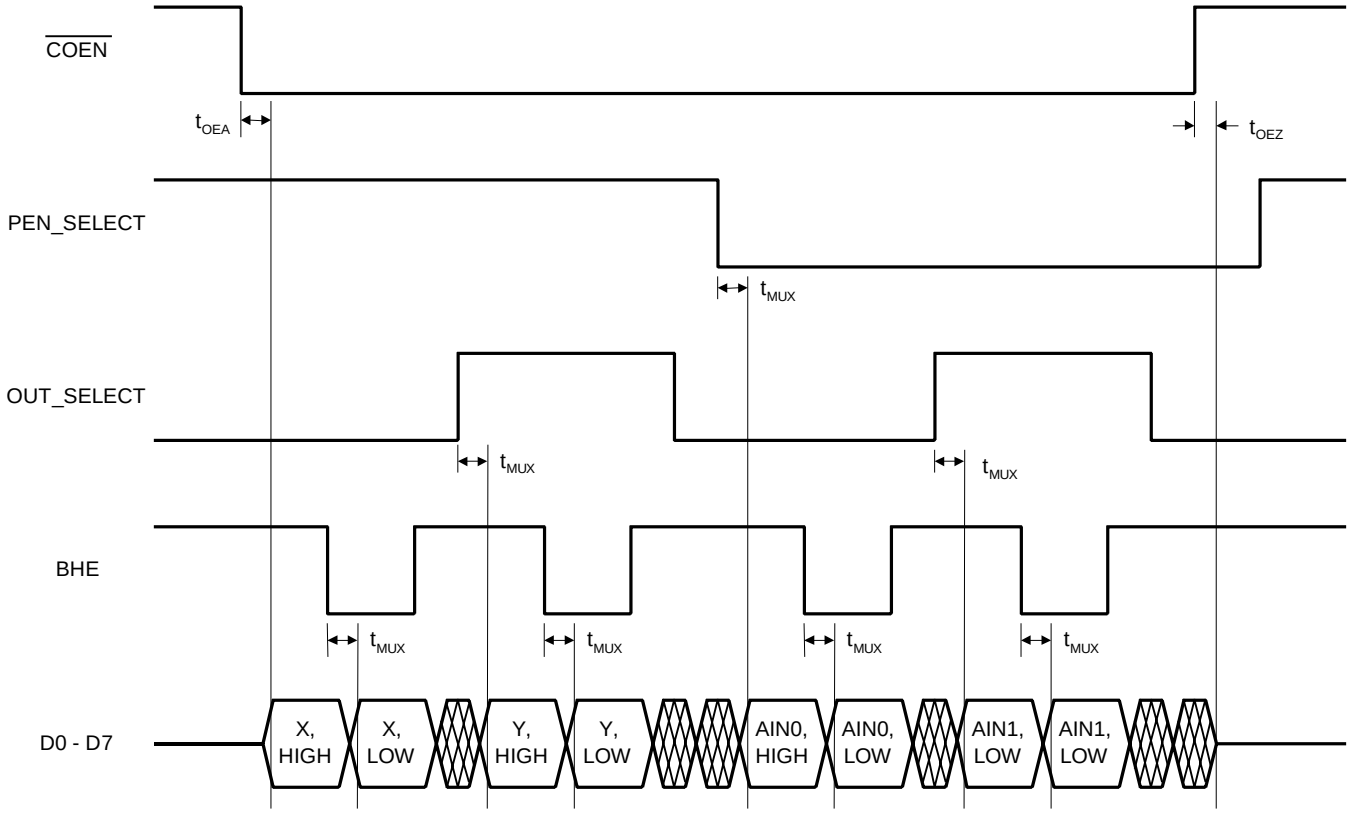
(0°C to 70°C; V_{CC}=5.0V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PFI Low to $\overline{PFO}$ Low	t_{PFD}			100	ns	
PFI High to $\overline{PFO}$ High	t_{PFU}			100	ns	
V_{CC} Detect to $\overline{RST}$ (V_{CC} Falling)	t_{RPD}			100	ns	
V_{CC} Detect to $\overline{RST}$ (V_{CC} Rising)	t_{RPU}		250		ms	16, 17
Reset Active Time	t_{RST}		250		ms	16
Pushbutton Debounce	PB_{DB}		250		ms	16
$\overline{ST}$ Pulse Width	t_{ST}	20			ns	
Chip Enable Propagation Delay to External SRAM	t_{CED}		8	15	ns	

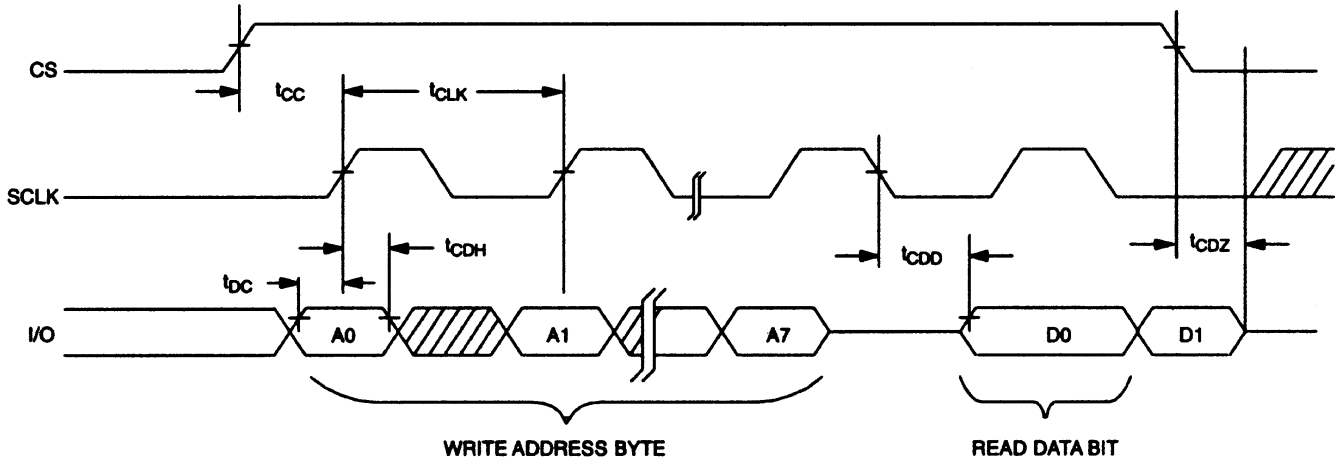
POWER-FAIL AND RESET
AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; V_{CC}=3.3V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PFI Low to $\overline{PFO}$ Low	t_{PFD}			200	ns	
PFI High to $\overline{PFO}$ High	t_{PFU}			200	ns	
V_{CC} Detect to $\overline{RST}$ (V_{CC} Falling)	t_{RPD}			200	ns	
V_{CC} Detect to $\overline{RST}$ (V_{CC} Rising)	t_{RPU}		250		ms	16, 17
Reset Active Time	t_{RST}		250		ms	16
Pushbutton Debounce	PB_{DB}		250		ms	16
$\overline{ST}$ Pulse Width	t_{ST}	40			ns	
Chip Enable Propagation Delay to External SRAM	t_{CED}		8	15	ns	

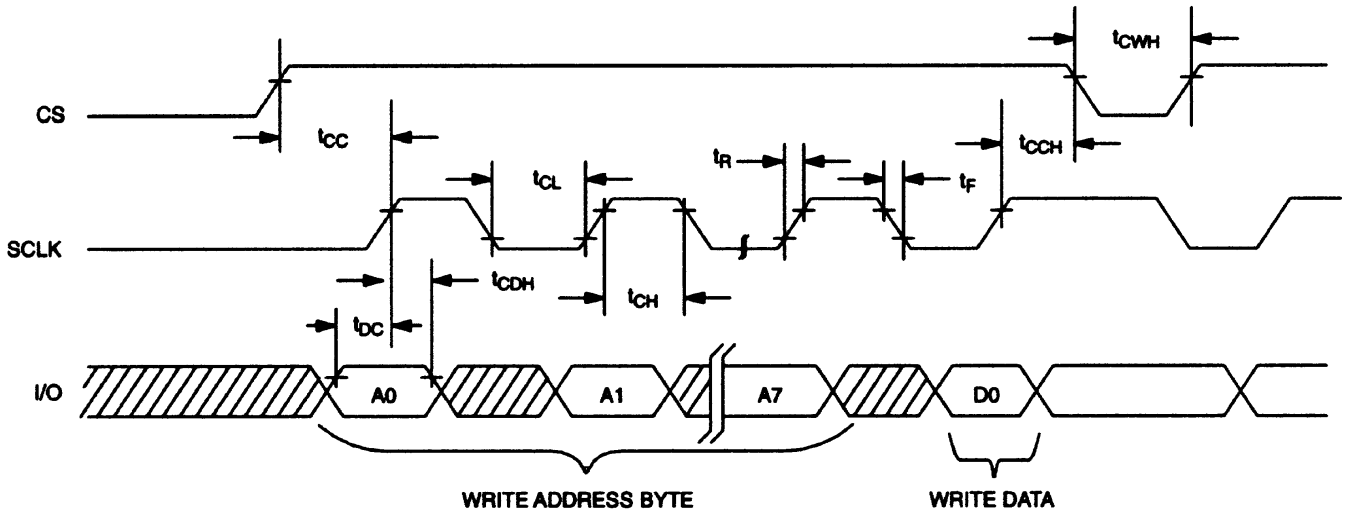
PARALLEL INTERFACE OUTPUT TIMING Figure 8



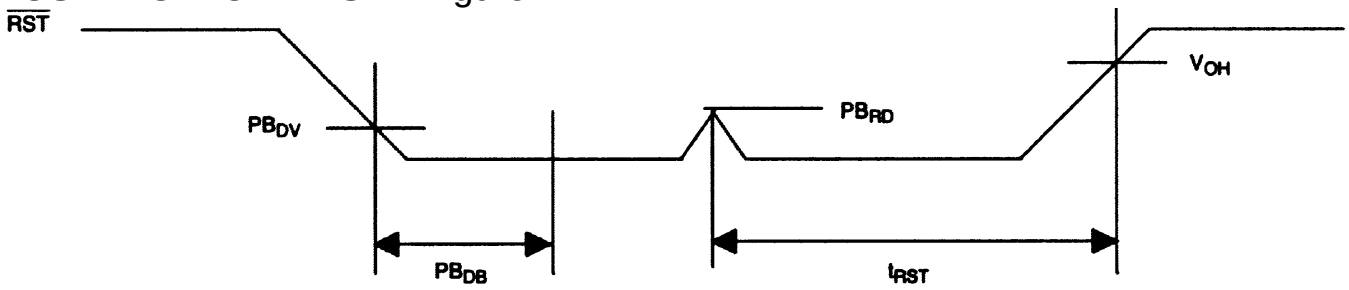
3-WIRE TIMING DIAGRAM: READ DATA Figure 9



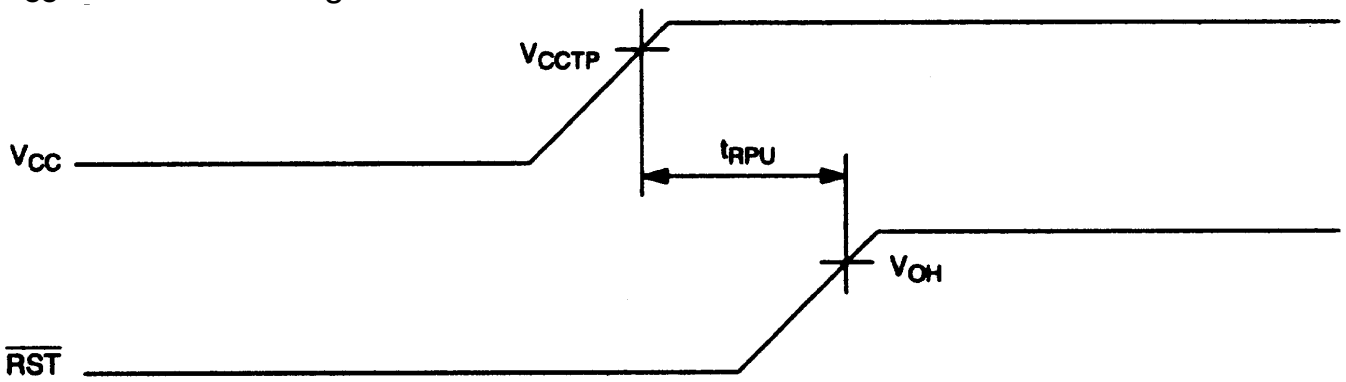
3-WIRE TIMING DIAGRAM: WRITE DATA Figure 10



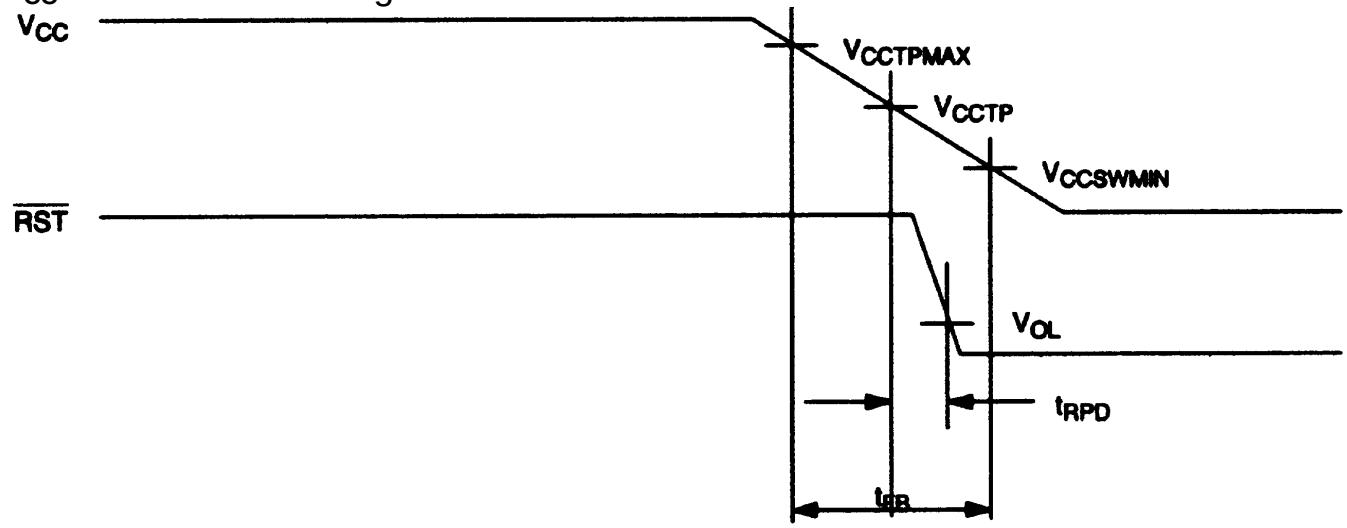
PUSH–BUTTON RESET Figure 11



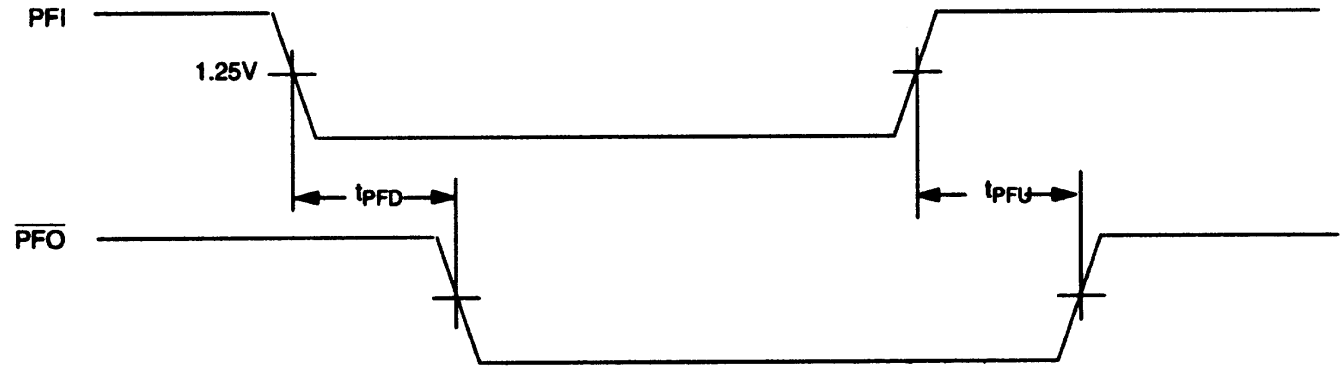
V_{CC} POWER–UP Figure 12



V_{CC} POWER–Down Figure 13



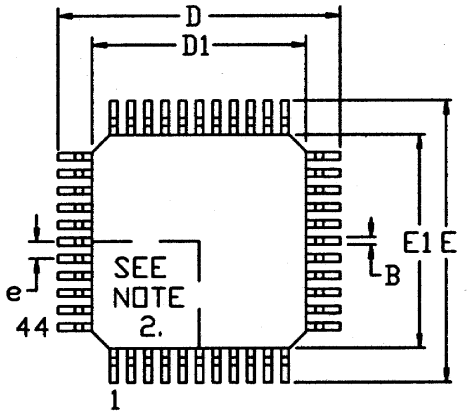
POWER–FAIL WARNING Figure 14

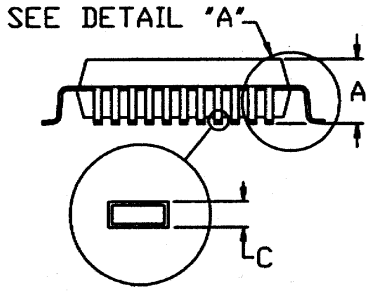


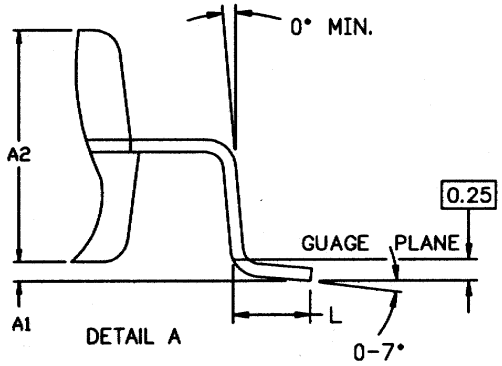
NOTES:

1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 0.4 mA at V_{CC}=3.0V, V_{OH}=V_{CC} for capacitive loads.
3. Logic zero voltages are specified at a sink current of 1.5 mA at V_{CC}=3.0, V_{OL}=GND for capacitive loads.
4. I_{CCA} is specified with outputs open, CS set to a logic 1, SCLK=500 kHz, oscillator enabled, A/D converter disabled, and no pen detected.
5. I_{CCS} is specified with CS, V_{CCO} open and I/O, SCLK at logic zero, A/D converter disabled, and no pen detected.
6. I_{AVDA} is specified with A/D converter enabled.
7. I_{AVDS} is specified with A/D converter disabled.
8. CS has a 40 kΩ pull–down resistor to ground.
9. Measured at V_{IH} =2.0V or V_{IL} =0.8V and 10 ns maximum rise and fall time.
10. Measured at V_{OH} =2.4V or V_{OL} =0.4V.
11. Load capacitance = 25 pF.
12. I_{CCO}=100 mA, V_{CC} > V_{CCTP}.
13. V_{CCO} switchover from V_{CC} to V_{BAT} occurs when V_{CC} drops below the lower of V_{CCSW} and V_{BAT}.
14. Current from V_{CC} input pin to V_{CCO} output pin.
15. Current from V_{BAT} input pin to V_{CCO} output pin.
16. Timebase is generated by the crystal oscillator. Accuracy of this time period is based on the 32 kHz crystal that is used. A typical crystal with a specified load capacitance of 6 pF will provide accuracy within ±100 ppm over the 0°C to 70°C temperature range. For greater accuracy see DS32kHz data sheet.
17. If the $\overline{EOSC}$ bit in the Control Register is set to a logic 1, t_{RPU} is equal to 250 ms plus the start–up time of the crystal oscillator.
18. V_{CC}=0V, V_{AVD}=0V, V_{BAT}=3.7V and oscillator enabled.
19. V_{CC}=0V, V_{AVD}=0V, V_{BAT}=3.7V and oscillator disabled.
20. I_{CCPD} is specified with outputs open, CS set to a logic 1, SCLK=500 kHz, oscillator enabled, A/D converter enabled, and pen detected.

DS1680 PACKAGE OUTLINE







DIM	MIN	MAX
A	-	2.45
A1	0.10	0.30
A2	1.95	2.10
D	13.65	14.30
D1	9.90	10.10
E	13.65	14.30
E1	9.90	10.10
L	0.63	1.03
e	0.80 BSC	
B	0.30	0.45
C	0.13	0.23

NOTES:

1. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH, BUT DO NOT INCLUDE MOLD PROTRUSION; ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE.

2. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

3. ALLOWABLE DAMPER PROTRUSION IS 0.08 MM TOTAL IN EXCESS OF THE B DIMENSION; AT MAXIMUM MATERIAL CONDITION. PROTRUSION NOT TO BE LOCATED ON LOWER RADIUS OF FOOT OF LEAD.

4. CONTROLLING DIMENSIONS: MILLIMETERS.